IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Divisional Application:

Shinji Sugatani and Satoshi Sekino

Serial No.: Filed Concurrently — Group Art Unit: Not Yet Assigned

Filed: August 6, 2003 — Examiner: Not Yet Assigned

For: MANUFACTURING METHOD OF SEMICONDUCTOR DEVICE AND SEMICONDUCTOR CHIP USING SOI SUBSTRATE

INFORMATION DISCLOSURE STATEMENT PURSUANT TO 37 CFR 1.97(b)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

August 6, 2003

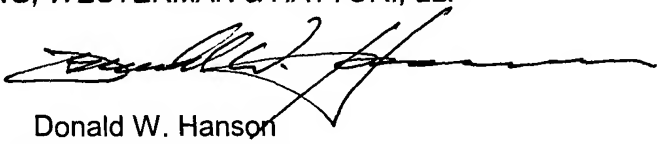
Sir:

This Information Disclosure Statement is being filed in order to comply with Applicant's duty of disclosure under 37 CFR 1.56. The documents listed on the Form PTO-1449 were made of record in parent application Serial No. 10/289,295.

The Commissioner is authorized to charge our Deposit Account No. 01-2340 for any fee which is deemed by the Patent and Trademark Office to be required to effect consideration of this statement.

Respectfully submitted,

ARMSTRONG, WESTERMAN & HATTORI, LLP



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PATENT TRADEMARK OFFICE

Enclosures: PTO-1449

INFORMATION DISCLOSURE STATEMENT PTO-1449	Atty. Docket No. **021331A**	Serial No. **New Application**
	Applicant(s): Shinji Sugatani and Satoshi Sekino	
	Filing Date: August 6, 2003	Group Art Unit: **Not Yet Assigned**

U.S. PATENT DOCUMENTS

Examiner Initial		Document No.	Name	Date	Class	Subclass	Filing Date (If appropriate)
_____	AA						
_____	AB						
_____	AC						
_____	AD						

FOREIGN PATENT DOCUMENTS

		Document No.	Date	Country	Translation (Yes or No)
_____	AE	9-246505	09/19/97	Japan	Yes - Abstract
_____	AF				
_____	AG				
_____	AH				
_____	AI				

OTHER DOCUMENTS

_____	AJ	H. Sayama et al.; "Effect of <100> Channel Direction for High Performance SCE Immune pMOSFET with Less Than 0.15μm Gate Length", 1999 International Electron Devices Meeting, Washington, D.C., December 5-8, 1999/Discussed in the specification
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Examiner	Date Considered